In the Title

Please change the title to: "INTEGRATED CIRCUIT WITH CAPACITORS HAVING A FIN STRUCTURE"

In the Specification:

Please amend Paragraph 0008 as follows:

Using a Fin field effect transistor (FinFET) based technology provides advantages toward high speed CMOS. FETs are the basic electrical devices of today's integrated circuits and are used in almost all types of integrated circuit design (i.e., microprocessors, memory, etc.). A FinFET is one type of FET that has been proposed to facilitate increased device performance. In a FinFET, a vertical "fin" shaped structure is defined to form the body of the transistor. Gates are then formed on one or both sides of the Fin. When gates are formed on both sides of the Fin, the transistor is generally referred to as a double gate FinFET. In particular, the use of the double gate suppresses Short Channel Effects (SCE), provides for lower leakage, and provides for more ideal switching behavior. In addition, the use of the double gate increases gate area, which allows the FinFET to have better current control, without increasing the gate length (also called "gate thickness") of the device. As such, the FinFET is able to have the current control of a larger transistor without requiring the device space of the larger transistor.

Please add the following paragraph after Paragraph 0020 and before "Detailed Description of the Invention":

FIG. 8 is a cross-sectional side view of a FinFET coupled to a capacitor shown in FIG. 7b.

Please amend Paragraph 0037 as follows:

Alternatively, for the exemplary purposes of this disclosure, in step 104, SIT may be used on

substrate 200 so that only narrow Fins may be formed from semiconductor layer 206, or SIT and CIT may be combined on substrate 200 so that both narrow and broad Fins may be formed from semiconductor layer 206. SIT allows the respective gate or electrode ~~length~~ thickness of the devices to have minimum feature size, while allowing the thickness of the Fin body to be much smaller than the respective gate or electrode ~~length~~ thickness. The Fin body thickness is determined by the image of a sidewall spacer, allowing the Fin body to be reliably formed at sub minimum feature size.

Please amend Paragraph 0043 as follows:

The final step is to pattern semiconductor layer 206 using the hard mask film 208 narrow lines as masks. This may be done using a suitable anisotropic etching process that etches semiconductor layer 206 stopping on buried insulator 204. Additionally, it is generally desirable to have the thickness of the narrow Fins (i.e., the thickness of semiconductor layer 206 portions) less than the gate or electrode structure ~~length~~ thickness. As the gate and electrode structure ~~length~~ thickness is generally made to minimum feature size, SIT is used to achieve the subminimum feature size of the narrow Fins. Therefore, as described above, the thickness of the sidewall spacer determines the thickness of the narrow Fin.

Please amend Paragraph 0054 as follows:

Thus, for example, in FIGS. 7a - 7b, nominal-voltage decoupling capacitor 214 and high-voltage decoupling capacitor 215 are depicted having a minimum of complexity. These depicted embodiments are at a stage of a process flow technique modified by an integration method of the

present invention for forming any number, combination, and/or type of inventive decoupling capacitors, CMOS FinFET's, and/or other devices on the same substrate in order to provide effective decoupling capacitance in an area-efficient manner. Particularly, wafer 202 is depicted with an overlying buried insulator 204. On top of buried insulator 204 are nominal-voltage decoupling capacitor 214 and high-voltage decoupling capacitor 215. Nominal-voltage decoupling capacitor 214 comprises narrow semiconductor layer 206 portion (the narrow Fin) with overlying thick hard mask film 208 narrow line. Insulator layers 210 are formed on opposing vertical sidewalls of the narrow Fin. Conductor layer 212 portion is structured adjacent insulator layer 210 portions and hard mask film 208 narrow line portion, thereby encapsulating the narrow Fin. High-voltage decoupling capacitor 215 comprises broad semiconductor layer 206 portion (the broad Fin) with overlying thick hard mask film 208 narrow line. Insulator layers 210 are formed on opposing vertical sidewalls of the broad Fin. Conductor layer 212 portion is structured adjacent hard mask film 208 broad line portion so that conductor layer 212 portion is within a thickness of the broad Fin. It is advantageous for the conductor layer 212 portion to partially overlay (or be within the thickness) of the broad Fin. If conductor layer 212 portion extended beyond the thickness of the broad Fin, thereby becoming additionally adjacent to a sidewall of the broad Fin, then a region of thin insulator on the sidewall would be exposed to high electric fields when using this decoupling capacitor at higher voltages. This would result in significantly higher leakage currents through the capacitor and in decreased reliability. For the capacitor 215, the thickness of the Fin 206 is T_{F1} and the thickness of the conductor layer 212 is T_{C1}. For the capacitor 214, the thickness of the Fin 206 is T_{F2} and the thickness of the conductor layer 212 is T_{C2}. As seen in FIGS. 7a-7b for the capacitor 215, the thickness of the conductor

layer 212 is within the thickness of the Fin 206, which means in FIGS. 7a-7b and in the claims that $T_{C1} \leq T_{F1}$ such that the sidewalls 11 and 12 of the conductor layer 212 are each disposed between the sidewalls 21 and 22 of the Fin 206 as shown. Also as seen in FIGS. 7a-7b for the capacitor 214, the thickness of the Fin 206 is within the thickness of the conductor layer 212, which means in FIGS. 7a-7b and in the claims that $T_{F2} \leq T_{C2}$ such that the sidewalls 41 and 42 of the Fin 206 are each disposed between the sidewalls 31 and 32 of the conductor layer 212 as shown. FIGS. 7a-7b also show that $T_{F1} \geq T_{F2}$..

Please insert the following paragraph between Paragraphs 0057 and 0058:

FIG. 8 depicts a cross-sectional side view of a FinFET 250 comprising a gate electrode 255 coupled to the high-voltage decoupling capacitor 215 of FIG. 7b. The gate electrode 255 of the FinFET 250 includes the same conductive material as does the electrode 212 of the capacitor 215, since both the gate electrode 255 of the FinFET 250 and the electrode 212 of the capacitor 215 were both formed from the conductor layer 212 of FIGS. 6a-6b as described *supra*. In FIG. 8, the FinFET 250 is disposed on the buried insulator 204 and is electrically coupled at a surface 251 of the gate electrode 255 by an interconnect 240 to the top surface 233 of the electrode 212 of the capacitor 215. Instead of the interconnect 240 being connected to the top surface 233 of the electrode 212, the interconnect 240 could alternatively have been connected to the side surface 231 of the electrode 212 or to the side surface 232 of the electrode 212. FIG. 8 also depicts interconnects 241 and 242 respectively connected to the side surfaces 231 and 232 of the electrode 212. While FIG. 8 depicts the FinFET 250 coupled to the capacitor 215, the FinFET 250 may be similarly coupled to the capacitor 214 of FIG. 7b.